LIST OF CURRENT CLAIMS

1. (Currently Amended) A method of designing a semiconductor integrated circuit, comprising ~~the following steps~~:

a first step for determining a number of clocks different in delay amount, which are used for verification of a circuit design of the semiconductor integrated circuit upon the circuit design thereof, and determining delays in the clocks on the basis of pre-set conditions for constraints of timings;

a second step for allocating clocks supplied to respective circuits; and

a third step for optimizing timings on the basis of a list obtained by the timing constraint conditions and the clock allocation, and determining whether results of analyses of the respective timings correspond to violation of the constraints of timings,

wherein the optimization of the timings is repeated according to the violation of the constraints of timings and ~~at least the first and second~~ the first, second, and third steps are directed to circuit design and are performed prior to performing a layout design of the semiconductor integrated circuit.

2. (Previously Presented) A method according to claim 1, further comprising performing a layout design including ~~the steps~~:

a fourth step for generating the clocks different in the delay amount for the verification of a layout design of the semiconductor integrated circuit;

a fifth step for adjusting skews for each of said clocks;

a sixth step for adjusting delays respectively included in the clocks to the determined clock delays upon the layout design, respectively; and

a seventh step for making an adjustment to a layout that satisfies the timing constraint conditions upon the layout design and determining whether analytical results of the respective timings correspond to the constraint violation,

wherein the layout adjustment is repeated according to the constraint violation.

3. (Previously Presented) A method according to claim 1, further comprising a step for adjusting the delay of each of the clocks again according to the constraint violation when the constraint violation exists in the third step.

4. (Previously Presented) A method according to claim 2, further comprising a step for adjusting delays set for said clocks according to the constraint violation when the constraint violation occurs in the seventh step.

5. (Previously Presented) A method according to claim 4, wherein adjusting the delays comprises adding an delay at a starting point where data is outputted, and determining the clock delays according to the difference between the added value and the cycle of the clock.